

PHD20N06T

N-channel TrenchMOS™ transistor

Rev. 01 — 22 February 2001

Product specification

1. Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™¹ technology.

Product availability:

PHD20N06T in SOT428 (D-PAK).

2. Features

- TrenchMOS™ technology
- Low on-state resistance
- Fast switching.

3. Applications

- Switched mode power supplies
- DC to DC converters
- General purpose switch.

4. Pinning information

Table 1: Pinning - SOT428 (D-PAK), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	<p>Top view MBK091</p> <p>SOT428 (D-PAK)</p>	<p>MBB076</p>
2	drain (d)		
3	source (s)		
mb	drain (d)		

1. TrenchMOS is a trademark of Royal Philips Electronics.



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5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)		–	55	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V}$	–	18	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$	–	51	W
T_j	junction temperature		–	175	°C
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 10\text{ A}$			
		$T_j = 25\text{ °C}$	65	77	mΩ
		$T_j = 175\text{ °C}$	–	154	mΩ

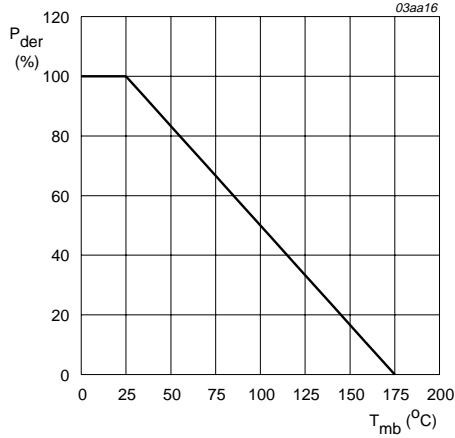
6. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

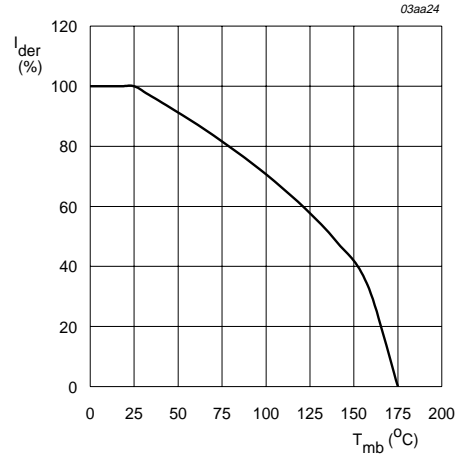
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)		–	55	V
V_{DGR}	drain-gate voltage (DC)	$R_{GS} = 20\text{ k}\Omega$	–	55	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ Figure 2 and 3	–	18	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V};$ Figure 2	–	13	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ Figure 3	[1]	73	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ Figure 1	–	51	W
T_{stg}	storage temperature		–55	+175	°C
T_j	operating junction temperature		–55	+175	°C
Source-drain diode					
I_{DR}	reverse drain current (DC)	$T_{mb} = 25\text{ °C}$	–	18	A
I_{DRM}	pulsed reverse drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s}$	–	73	A
Avalanche ruggedness					
W_{DSS}	non-repetitive avalanche energy	unclamped inductive load; $I_D = 6\text{ A};$ $V_{DS} \leq 55\text{ V}; V_{GS} = 10\text{ V}; R_{GS} = 50\text{ }\Omega;$ starting $T_j = 25\text{ °C}$	–	36	mJ

[1] I_{DM} is limited by chip, not package.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

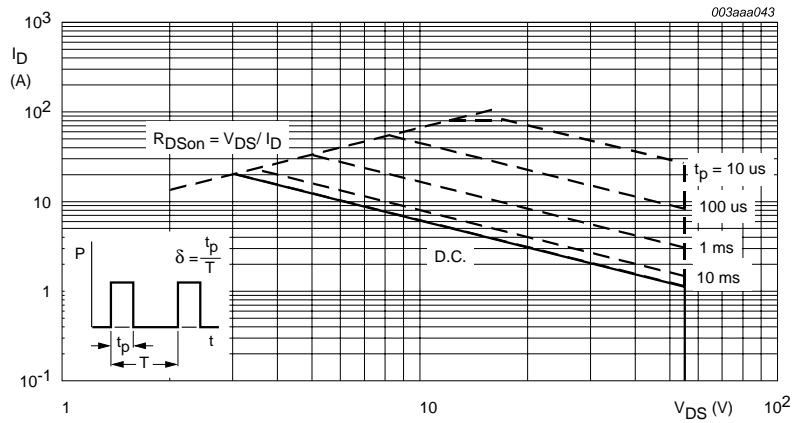
Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$V_{GS} \geq 4.5 \text{ V}$$

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}C$; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint, FR4 board	71.4	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	2.9	K/W

7.1 Transient thermal impedance

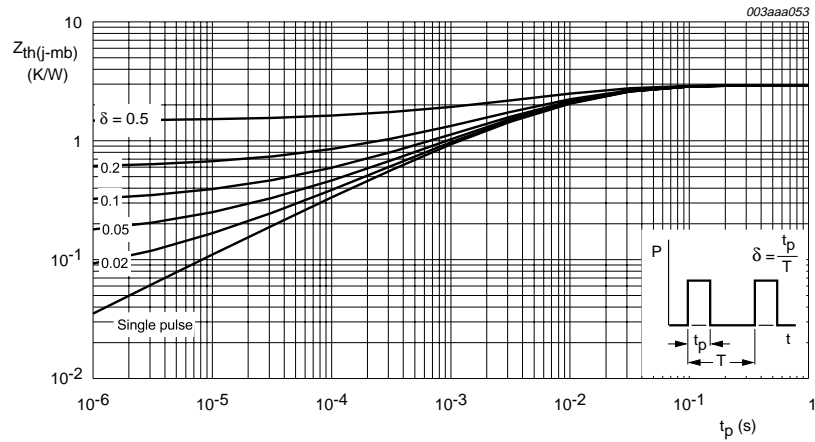


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

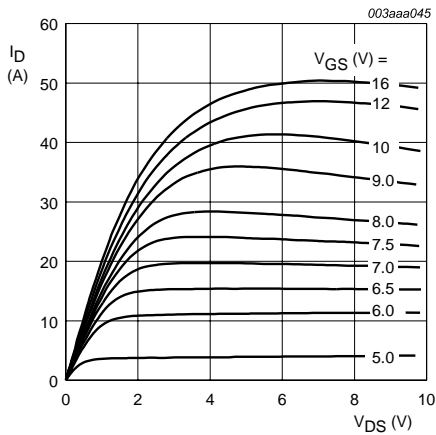
8. Characteristics

Table 5: Characteristics
T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 0.25 mA; V _{GS} = 0 V T _j = 25 °C	55	–	–	V
		T _j = –55 °C	50	–	–	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; Figure 9				
		T _j = 25 °C	2	3	4	V
		T _j = 175 °C	1	–	–	V
		T _j = –55 °C	–	–	4.4	V
I _{DSS}	drain-source leakage current	V _{DS} = 55 V; V _{GS} = 0 V T _j = 25 °C	–	0.05	10	μA
		T _j = 175 °C	–	–	500	μA
I _{GSS}	gate-source leakage current	V _{GS} = ±20 V; V _{DS} = 0 V	–	2	100	nA
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 10 A; Figure 7 and 8				
		T _j = 25 °C	–	65	77	mΩ
		T _j = 175 °C	–	–	154	mΩ
Dynamic characteristics						
Q _{g(tot)}	total gate charge	I _D = 25 A; V _{DD} = 44 V;	–	11	–	nC
Q _{gs}	gate-source charge	V _{GS} = 10 V; Figure 14	–	3	–	nC
Q _{gd}	gate-drain (Miller) charge		–	6	–	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V;	–	316	422	pF
C _{oss}	output capacitance	f = 1 MHz; Figure 12	–	92	110	pF
C _{rss}	reverse transfer capacitance		–	64	87	pF
t _{d(on)}	turn-on delay time	V _{DD} = 30 V; R _L = 1.2 Ω;	–	10	–	ns
t _r	rise time	V _{GS} = 10 V; R _G = 10 Ω;	–	50	–	ns
t _{d(off)}	turn-off delay time		–	70	–	ns
t _f	fall time		–	40	–	ns
L _d	internal drain inductance	measured from drain lead from package to centre of die	–	2.5	–	nH
L _s	internal source inductance	measured from source lead from package to source bond pad	–	7.5	–	nH

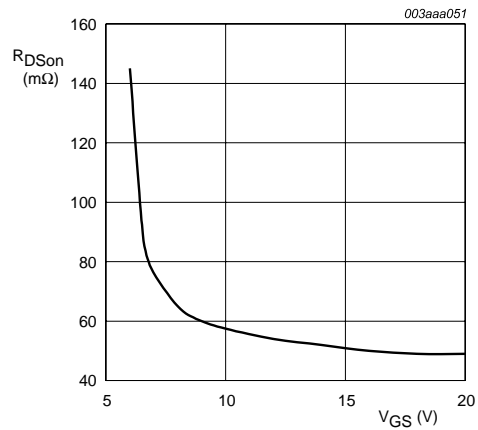
Table 5: Characteristics...continued
T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 10 A; V _{GS} = 0 V; Figure 15	–	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = –100 A/μs;	–	32	–	ns
Q _r	recovered charge	V _{GS} = –10 V; V _{DS} = 30 V	–	120	–	nC



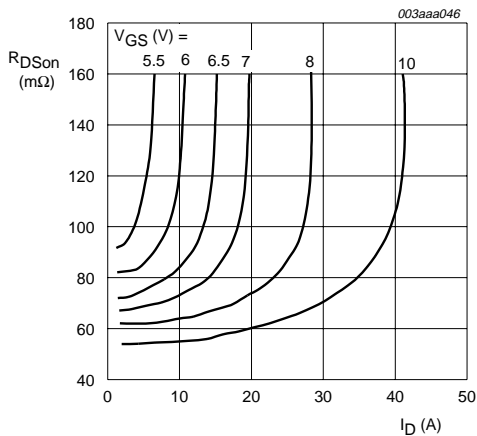
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



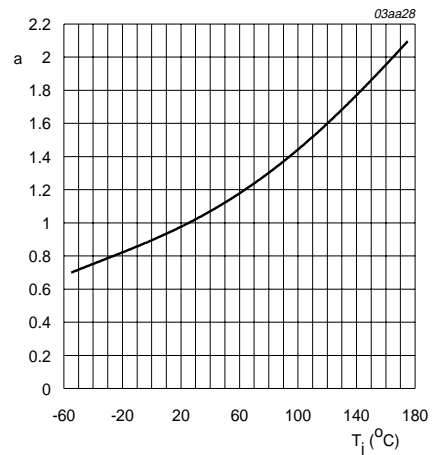
T_j = 25 °C; I_D = 10 A

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.



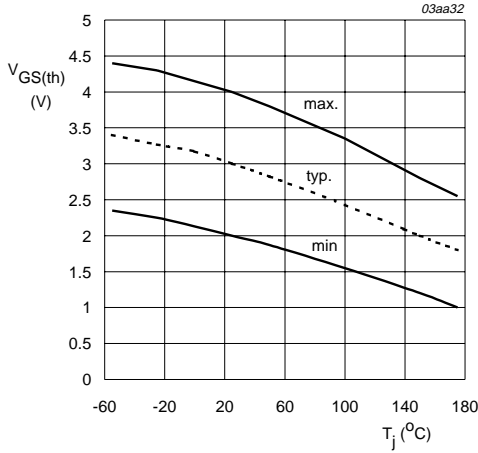
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



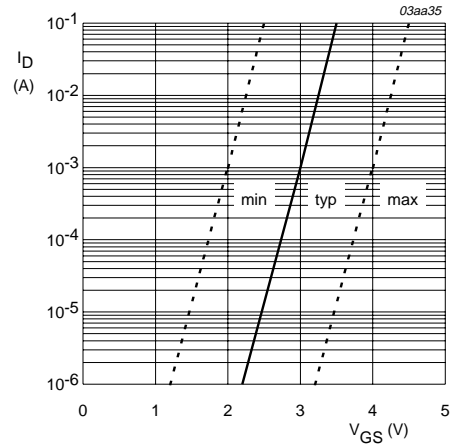
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^{\circ}C)}}$$

Fig 8. Normalized drain source on-state resistance factor as a function of junction temperature.



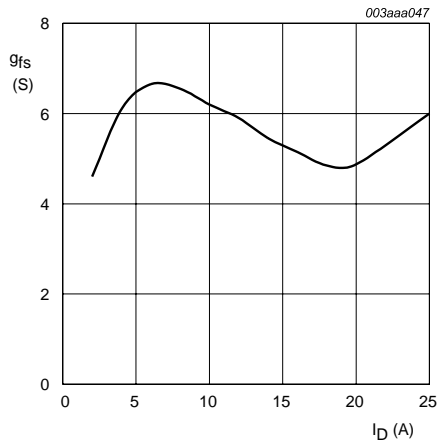
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



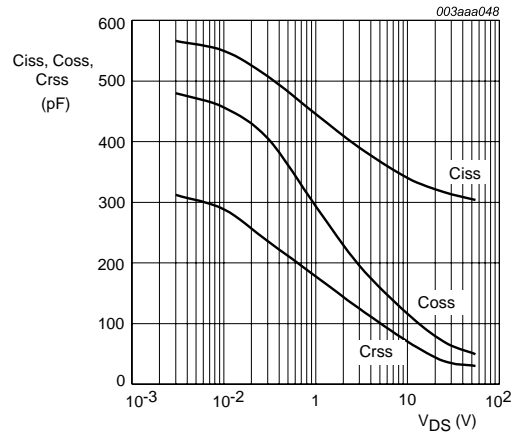
$T_j = 25 \text{ °C}; V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



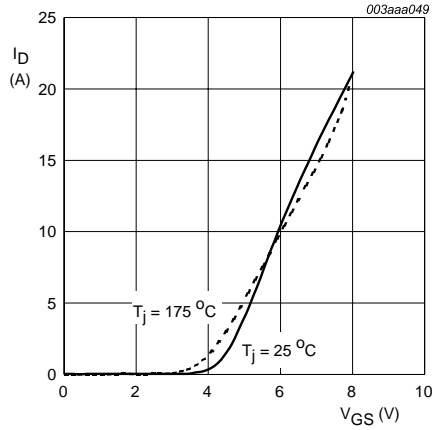
$T_j = 25 \text{ °C}; V_{DS} = 25 \text{ V}$

Fig 11. Forward transconductance as a function of drain current; typical values.



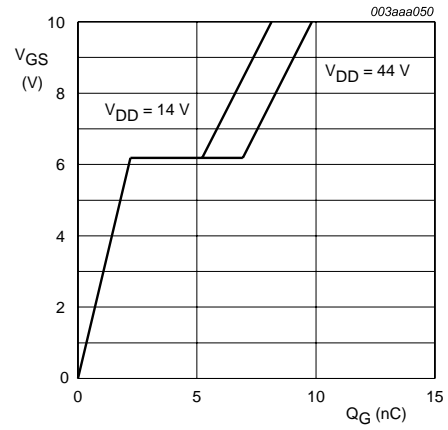
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



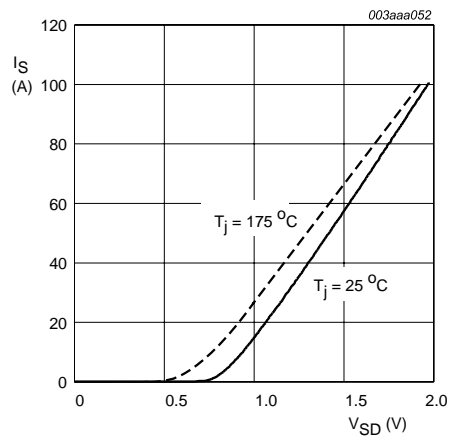
$V_{DS} = 25\text{ V}$

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



$T_j = 25\text{ }^\circ\text{C}$; $I_D = 10\text{ A}$

Fig 14. Gate-source voltage as a function of gate charge; typical values.



$V_{GS} = 0\text{ V}$

Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

9. Package outline

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped)

SOT428

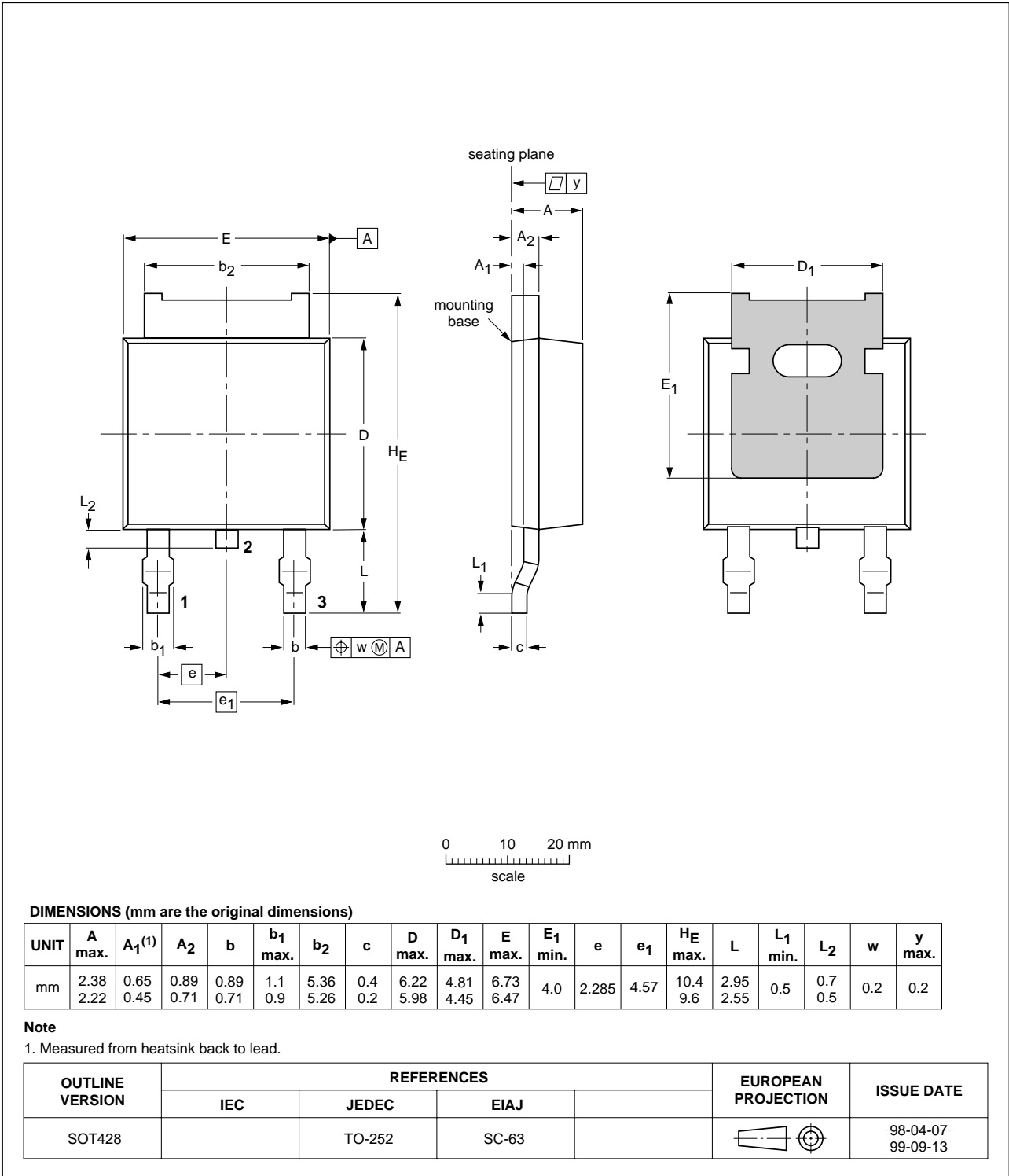


Fig 16. SOT428 (D-PAK).

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20010222	-	Product specification; initial version.

11. Data sheet status

Datasheet status	Product status	Definition ^[1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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